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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,963	04/23/2001	Sangki Hong	CS99-210	4495

28112 7590 06/14/2005

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/839,963	HONG ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,9-12,15 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,9-12,15 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. (U.S. 4,536,951), Ye et al. (U.S. 6,080,529), Huang et al. (U.S. 6,180,509 B1) and Liu et al. (U.S. 5,693,568).

In reference to claims 1 and 2, Rhodes et al. (Figs.1-5) teach a method of forming interconnects including providing a semiconductor substrate (4); depositing a first metal layer (2) overlying said semiconductor substrate (4); depositing an etch stop layer (6) overlying said first metal layer (2) wherein said etch stop layer (6) comprises a chromium or a titanium film; depositing a second metal layer (8) overlying said first metal layer (2), wherein said first (2) and second (8) are made of aluminum; etching through said second metal layer (8), said etch stop layer (6) and said first metal layer (2) to form connective lines; thereafter etching through said second metal layer (8) down to the etch stop layer (6) forming vias; thereafter depositing a dielectric layer (12) overlying said vias, said connective lines and said semiconductor substrate (4); and etching down said dielectric layer (12) to complete said self-aligned interconnect structure (column 2, line 44 – column 4, line 33).

Rhodes et al. fail to teach wherein said etch stop layer includes a tantalum material. However, Ye et al. (Figs.2A-3G) in a related method to pattern metal layers teach depositing an etch stop layer (218) over a metal layer (216) comprising copper or aluminum; wherein said etch stop layer comprises a material selected from the group comprising titanium, and a tantalum containing material (column 12, line 40 – column 15, line 25). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al. and Ye et al. to using tantalum material in the etch stop layer of Rhodes et al. according to the teachings of Ye et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etch stop forming step of Rhodes et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al. and Ye et al. to enable the formation of the etch stop layer of Rhodes et al. to be performed according to the teachings of Huang et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etch stop formation step of Rhodes et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Rhodes et al. and Ye et al. teach using antireflective layers such as titanium nitride and tantalum nitride (Ye et al., column 14, lines 8 – 21). Still, the combined teachings of Rhodes et al. and Ye et al. fail to expressly teach

depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer. However, Huang et al. (Figs.1-6) in a related method to pattern metal layers teach forming an etch stop layer titanium nitride on a second metal layer (Huang et al. column 6, lines 43 – 48). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Rhodes et al. and Ye et al. with Huang et al. to enable forming a titanium nitride layer on said second metal layer of the combination of Rhodes et al. and Ye et al., since it can be used to protect underlying layers as an etching stop layer as disclosed by Huang et al. but also as an antireflective layer as disclosed by Ye et al.

The combined teachings of Rhodes et al., Ye et al. and Huang et al. fail to teach polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device. However, Liu et al. (Figs.1-9) in a related method to form self-aligned anti-via interconnects teach depositing dielectric layer (51) over a patterned via (40); and polishing down said dielectric layer (50), completing said anti-via interconnect structure (column 7, lines 51 – 55). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al., Ye et al. and Huang et al. with the teachings of Liu et al. enable the removing step of the combined teachings of Rhodes et al., Ye et al. and Huang et al. to be performed according to the teachings of Liu et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of the combined teachings of Rhodes et al., Ye et al. and Huang et al. and art recognized suitability for

an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 3, the combined teachings of Rhodes et al., Ye et al., Huang et al. and Liu et al. teach wherein said semiconductor substrate comprises semiconductor devices in and on a silicon substrate covered by an insulating layer (Rhodes et al., column 2, lines 44 – 45 and Liu et al, column 6, lines 39 – 53).

In reference to claim 6, the combined teachings of Rhodes et al., Ye et al., Huang et al. and Liu et al. substantially teach all aspects of the invention but fail to disclose wherein said dielectric layer is deposited to a thickness between about 5,000 Angstroms and 20,000 Angstroms. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

3. Claims 9-12, 15 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. (U.S. 4,536,951), Ye et al. (U.S. 6,080,529), Huang et al. (U.S. 6,180,509 B1) and Liu et al. (U.S. 5,693,568) and Pangrle et al. (U.S. 6,713,382 B1).

In reference to claims 9, 10, 15, 18, 19, Rhodes et al. (Figs.1-5) teach a method of forming interconnects including providing a semiconductor substrate (4); depositing a first metal layer (2) overlying said semiconductor substrate (4); depositing an etch stop layer (6) overlying said first metal layer (2) wherein said etch stop layer (6) comprises a chromium or a titanium film; depositing a second metal layer (8) overlying said first metal layer (2), wherein said first (2) and second (8) are made of aluminum; etching through said second metal layer (8), said etch stop layer (6) and said first metal layer (2) to form connective lines; thereafter etching through said second metal layer (8) down to the etch stop layer (6) forming vias; thereafter depositing a dielectric layer (12) overlying said vias, said connective lines and said semiconductor substrate (4); and etching down said dielectric layer (12) to complete said self-aligned interconnect structure (column 2, line 44 – column 4, line 33).

Rhodes et al. fail to teach wherein said etch stop layer includes a tantalum material. However, Ye et al. (Figs.2A-3G) in a related method to pattern metal layers teach depositing an etch stop layer (218) over a metal layer (216) comprising copper or aluminum; wherein said etch stop layer comprises a material selected from the group comprising titanium, and a tantalum containing material (column 12, line 40 – column 15, line 25). It would have been within the scope of one of ordinary skill in the art to

combine the teachings of Rhodes et al. and Ye et al. to using tantalum material in the etch stop layer of Rhodes et al. according to the teachings of Ye et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etch stop forming step of Rhodes et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al. and Ye et al. to enable the formation of the etch stop layer of Rhodes et al. to be performed according to the teachings of Huang et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etch stop formation step of Rhodes et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Rhodes et al. and Ye et al. teach using antireflective layers such as titanium nitride and tantalum nitride (Ye et al., column 14, lines 8 – 21). Still, the combined teachings of Rhodes et al. and Ye et al. fail to expressly teach depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer. However, Huang et al. (Figs.1-6) in a related method to pattern metal layers teach forming an etch stop layer titanium nitride on a second metal layer (Huang et al. column 6, lines 43 – 48). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Rhodes et al. and Ye et al. with Huang et al. to enable forming a titanium nitride layer on

said second metal layer of the combination of Rhodes et al. and Ye et al., since it can be used to protect underlying layers as an etching stop layer as disclosed by Huang et al. but also as an antireflective layer as disclosed by Ye et al.

The combined teachings of Rhodes et al., Ye et al. and Huang et al. fail to teach polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device. However, Liu et al. (Figs.1-9) in a related method to form self-aligned anti-via interconnects teach depositing dielectric layer (51) over a patterned via (40); and polishing down said dielectric layer (50), completing said anti-via interconnect structure (column 7, lines 51 – 55). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al., Ye et al. and Huang et al. with the teachings of Liu et al. enable the removing step of the combined teachings of Rhodes et al., Ye et al. and Huang et al. to be performed according to the teachings of Liu et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of the combined teachings of Rhodes et al., Ye et al. and Huang et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Rhodes et al., Ye et al., Huang et al. and Liu et al. teach using parylene as an interlayer dielectric film (Rhodes et al., column 3, lines 47 – 50), but fail to teach wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous

materials, PPXC polymer (poly(chloro-p-xylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene). However, Pangrle et al. (Fig.2B) teach a method of forming interconnects including forming a dielectric layer (114) used as an intermetal dielectric), wherein said dielectric layer is formed form low-k materials such as SiOF, parylene and porous such as siloxanes and silsesquioxanes (column 3, lines 24 – 55 and column 7, lines 55 – 67).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Rhodes et al., Ye et al., Huang et al. and Liu et al. with Pangrle et al. to enable the dielectric forming step of Rhodes et al., Ye et al., Huang et al. and Liu et al. to be performed according to the teachings of Pangrle et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed dielectric forming step of Rhodes et al., Ye et al., Huang et al. and Liu et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 11, 12, 20 and 21, the combined teachings of Rhodes et al., Ye et al., Huang et al., Liu et al. and Pangrle et al. substantially teach all aspects of the invention but fail to disclose wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise

critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Response to Arguments

4. Applicant's arguments filed 03/25/2005 have been fully considered but they are not persuasive.

In regards to the Ye et al. reference, Applicants argue, "...Ye et al. does no teach or suggest a method for using these layers (tantalum nitride) as an etching stop...". In response to these arguments, Ye et al. in Figs. 2B, 3B and 3E and related text teach etching down to tantalum nitride layers and it is not affected by an etching reaction (Ye et al., column 15, lines 6 – 18). Therefore, the tantalum nitride layers of Ye et al. do behave as etch stop layers as claimed.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
June 7, 2005

George Fourson
Primary Examiner